This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1. (original) A multi-package module, comprising
a module substrate,
a processor mounted on a portion of a first surface of the module substrate, and
a memory package stack disposed over a portion of the module substrate adjacent the portion to which the processor is mounted.

2. (original) The multi-package module of claim 1 wherein the processor is mounted onto a portion of the module substrate surface about the center, and wherein the memory package stack is disposed in part over a portion of the module substrate surface partly to one side of the portion to which the processor is mounted.

3. (original) The multi-package module of claim 1 wherein the memory package stack is mounted onto a portion of the module substrate adjacent the portion to which the processor is mounted.

4. (original) The multi-package module of claim 1 wherein the memory package stack is mounted onto a portion of the processor and wherein the memory package stack is situated in part over a portion of the module substrate surface partly to one side of the processor mounting portion.

5. (original) The multi-package module of claim 1 wherein the processor comprises a CPU.

6. (original) The multi-package module of claim 1 wherein the processor comprises a GPU.

7. (original) The multi-package module of claim 1 wherein the processor comprises an ASIC.

8. (original) The multi-package module of claim 1 wherein the memory package stack comprises a first package affixed onto a first surface of a package stack substrate and a second package affixed onto a second surface of the package stack substrate.

9. (original) The multi-package module of claim 8 wherein the first package is a BGA package.

10. (original) The multi-package module of claim 8 wherein the first package is a LGA package.

11. (original) The multi-package module of claim 1, comprising a plurality of memory package stacks disposed over portions of the module substrate adjacent the portion to which the processor is mounted.

12. (original) The multi-package module of claim 2, comprising a plurality of memory package stacks each disposed in part over a portion of the module substrate surface partly to one side of the portion to which the processor is mounted.

13. (original) The multi-package module of claim 3, comprising a plurality of memory package stacks mounted onto portions of the module substrate adjacent the portion to which the processor is mounted.

14. (original) The multi-package module of claim 4, comprising a plurality of memory package stacks each mounted onto a portion of the processor and each being situated in part over a portion of the module substrate surface partly to one side of the processor mounting portion.

15. (original) The multi-package module of claim 11 wherein each memory package stack comprises a first package affixed onto a first surface of a package stack substrate and a second package affixed onto a second surface of the package stack substrate.

16. (original) The multi-package module of claim 15 wherein the plurality of memory package stacks comprise a memory package assembly, and wherein a common memory package assembly substrate comprises the package stack substrate for each of the plurality of memory package stacks.

17. (original) The multi-package module of claim 16 wherein the common memory assembly substrate spans the portion of the module substrate onto which the processor is mounted.

18. (original) The multi-package module of claim 16 wherein an opening is provided in the common memory assembly substrate over the processor.

19. (original) The multi-package module of claim 18 wherein a heat slug is mounted onto the processor, and the opening in the common memory assembly substrate accommodates the heat slug.

20. (original) The multi-package module of claim 19 wherein the heat slug occupies the volume between a top surface of the processor and an upper limit of the module.

21. (original) The multi-package module of claim 20 wherein a heat spreader is mounted onto a top surface of the heat slug.

22. (original) The multi-package module of claim 9 wherein an array of balls provides for electrical interconnection of each BGA memory package to a surface of the memory stack substrate.

23. (original) The multi-package module of claim 22 wherein an array of bumps provides for electrical interconnection of each BGA memory package to a surface of the memory stack substrate.

24. (original) The multi-package module of claim 9 wherein an upper BGA package in the stack is connected to an upper surface of the memory stack substrate and a lower BGA package in the stack is inverted and connected to a lower surface of the memory stack substrate.

25. (original) The multi-package module of claim 10 wherein z-interconnection between the LGA memory packages and the module substrate is made by wire bonding between each LGA memory package substrate and the module substrate.

26. (original) The multi-package module of claim 10 wherein the LGA memory packages in the stack are stacked in like orientation, and are separated by spacers to provide relief for z-interconnect wire bond loops between a lower package in the stack and the module substrate.

27. (original) The multi-package module of claim 10 wherein each LGA memory package in the stack is electrically connected to the memory stack substrate by wire bonding, and the z-interconnect between the memory package and the module substrate is made by wire bonding between the memory stack substrate and the module substrate.

28. (original) The multi-package module of claim 10 wherein a lower LGA package in the stack is affixed to and is wire bond connected to a lower surface of the memory stack substrate and an upper LGA package in the stack is inverted and affixed to and is wire bond connected to an upper surface of the memory stack substrate.

29. (original) A multi-package module comprising

a module substrate,

a processor mounted on a portion of a first surface of the module substrate, and

a plurality of memory package stacks disposed in part over a portion of the module substrate adjacent the portion to which the processor is mounted.

30. (original) The multi-package module of claim 29 wherein the processor is mounted onto a portion of the module substrate surface about the center, and wherein the memory package stacks

are disposed in part over portions of the module substrate surface partly adjacent the portion to which the processor is mounted.

31. (original) The multi-package module of claim 29 wherein the memory package stacks are mounted onto portions of the module substrate adjacent the portion to which the processor is mounted.

32. (original) The multi-package module of claim 29 wherein the memory package stacks are mounted onto a portion of the processor and wherein the memory package stacks are situated in part over portions of the module substrate surface partly adjacent the processor mounting portion.

33. (original) The multi-package module of claim 29 wherein the processor comprises a CPU.

34. (original) The multi-package module of claim 29 wherein the processor comprises a GPU.

35. (original) The multi-package module of claim 29 wherein the processor comprises an ASIC.

36. (original) The multi-package module of claim 29 wherein each memory package stack comprises a first package affixed onto a first surface of a package stack substrate and a second package affixed onto a second surface of the package stack substrate.

37. (original) The multi-package module of claim 36 wherein the first package is a BGA package.

38. (original) The multi-package module of claim 36 wherein the first package is a LGA package.

39. (original) The multi-package module of claim 29 wherein each memory package stack comprises a first package affixed onto a first surface of a package stack substrate and a second package affixed onto a second surface of the package stack substrate.

40. (original) The multi-package module of claim 39 wherein the plurality of memory package stacks comprise a memory package assembly, and wherein a common memory package assembly substrate comprises the package stack substrate for each of the plurality of memory package stacks.

41. (original) The multi-package module of claim 40 wherein the common memory assembly substrate spans the portion of the module substrate onto which the processor is mounted.

42. (original) The multi-package module of claim 41 wherein an opening is provided in the common memory assembly substrate over the processor.

43. (original) The multi-package module of claim 42 wherein a heat slug is mounted onto the processor, and the opening in the common memory assembly substrate accommodates the heat slug.

44. (original) The multi-package module of claim 43 wherein the heat slug occupies the volume between a top surface of the processor and an upper limit of the module.

45. (original) The multi-package module of claim 44 wherein a heat spreader is mounted onto a top surface of the heat slug.

46. (original) The multi-package module of claim 40 wherein the memory packages comprise BGA memory packages and wherein an array of balls provides for electrical interconnection of each BGA memory package to a surface of the common memory assembly substrate.

47. (original) The multi-package module of claim 40 wherein the memory packages comprise BGA memory packages and an array of bumps provides for electrical interconnection of each BGA memory package to a surface of the common memory assembly substrate.

48. (original) The multi-package module of claim 40 wherein the memory packages comprise BGA packages and wherein an upper BGA package in the stack is connected to an upper surface of the common memory assembly substrate and a lower BGA package in the stack is inverted and connected to a lower surface of the common memory assembly substrate.

49. (original) The multi-package module of claim 29 wherein the memory packages comprise LGA memory packages.

50. (original) The multi-package module of claim 49 wherein z-interconnection between the LGA memory packages and the module substrate is made by wire bonding between each LGA memory package substrate and the module substrate.

51. (original) The multi-package module of claim 49 wherein the LGA memory packages in the stack are stacked in like orientation, and are separated by spacers to provide relief for z-interconnect wire bond loops between a lower package in the stack and the module substrate.

52. (original) The multi-package module of claim 40 wherein each LGA memory package is electrically connected to the common memory assembly substrate by wire bonding, and the z-interconnect between the memory package assembly and the module substrate is made by wire bonding between the common memory assembly substrate and the module substrate.

53. (original) The multi-package module of claim 40 wherein a lower LGA package is affixed to and is wire bond connected to a lower surface of the common memory assembly substrate and an upper LGA package is inverted and affixed to and is wire bond connected to an upper surface of the common memory assembly substrate.

54. (original) The multi-package module of claim 31, comprising two said memory package stacks, one each disposed on opposite sides of the processor.

55. (original) The multi-package module of claim 31, comprising four said memory package stacks, two each disposed on opposite sides of the processor.

56. (withdrawn) A method for making a multi-package module including a processor and a plurality of memory packages, comprising

providing a module substrate, a processor, and a plurality of memory package stacks;

mounting the processor on a first surface of the substrate;

mounting the memory packages over the first surface of the substrate; and

making z-interconnection of the memory packages and the module substrate by forming wire bonds between the memory packages and the module substrate.

57. (withdrawn) The method of claim 56 wherein providing a plurality of memory package stacks comprises attaching memory packages to a plurality of memory stack substrates, and making z-interconnection comprises forming wire bonds between the memory stack substrates and the module substrate.

58. (withdrawn) The method of claim 56 wherein providing a plurality of memory package stacks comprises attaching memory packages to a common memory assembly substrate, and making z-interconnection comprises forming wire bonds between the common memory assembly substrate and the module substrate.